REMARKS

Claims 1-27 are pending in the above-referenced patent application. (Claims 28-42 have been withdrawn from consideration by the Examiner and have been canceled in this Reply).

Claims 1-27 were rejected. Specifically, Claims 1, 3, 5-10, 12-27 were rejected under 35 U.S.C. 103(a) as being unpatentable over US APP 2002/0081873 to Harris et al ("Harris") in view of USPN 6,763,402 to Talati. Claims 2, 4, 11 were rejected under 35 U.S.C. 103(a) as being unpatentable over Harris, in view of Talati and further in view of USPN 6,131,135 to Abramson et al. ("Abramson").

All of the rejections are respectfully traversed because, for at lese the following reasons, the references, alone or in combination, do not disclose all of the limitations of the claims as amended.

As per **Claim 1**, Harris does not disclose plurality of bridges per USB controller. As the Examiner also states, unlike the claimed invention herein, Harris does not disclose multiple bridges connected to a USB controller. Harris only mentions and shows that a mass storage device motherboard or secondary board includes a bridging Circuit. One mass storage device, is connected to one bridge. Further, Applicant respectfully disagrees with the Examiner's statement that a USB controller, as claimed, is inherent in Harris. Harris does not show a USB controller as claimed, and the Examiner has not shown that a USB controller of the type claimed herein is used in Harris. Further, Harris does not disclose that its bridge provides protocol conversion that is even useable in a system were multiple bridges are connected to a USB controller as claimed herein.

In all of the detailed diagrams of the invention of Harris, there is mention of a USB controller being used. Further, Harris does not disclose a USB controller, wherein the USB-to-IDE bridges are connected to the USB controller, whereby the processor can communicate with the IDE devices via the USB controller. Nor does Harris mention a USB controller that can be connected to

multiple USB-to-IDE bridges for communication therewith. Nor does Harris disclose that the USB-to-IDE bridges are connected to the USB controller via a USB bus.

Harris teaches away from connecting multiple bridges to a USB Controller. The Examiner relies on Talati (Fig. 1) to disclose plurality of bridges to connect plurality of IDE devices. Then, the Examiner concludes that it would have been obvious to use plurality of USB-to-IDE bridges connected to a respective IDE device since this would enable multiple IDE devices to be connected to the host using the USB interface and increase storage capacity. The Examiner also interprets the claimed limitation as mere duplication of working parts of the USB-to-IDE bridge, which is coupled to an IDE device, requiring only routine skill in the art. Applicant respectfully disagrees.

The Examiner seems to suggest that using multiple bridges allows more IDE devices to be connected in Harris' USB system. However, that is true when multiple devices are connected to each bridge, not when only one device is connected to each bridge as claimed herein. According to the claimed invention, each IDE device is connected to the USB Controller via a corresponding bridge. Each bridge connects one IDE device to the USB controller. The function of each bridge is protocol conversion such that the corresponding IDE device can communicate with the USB controller. The function of each bridge is not to connect multiple IDE devices to a controller, and indeed each bridge does not connect multiple IDE devices to the USB controller.

Talati (Fig. 1, relied on by the Examiner) does not disclose plurality of bridges to connect plurality of IDE devices to a USB controller, as claimed. In Talati, Fig. 1 only shows DSD devices 110-112 connected to respective bridges 120-122, and bridges 120-122 connected to PHY controller 102. However, there is no disclosure in Talati that the bridges are USB-to-IDE bridges. Indeed, there is no mention of USB in Talati. Further, there is no mention that the PHY controller 102 is a USB controller as claimed herein. Nor does Talati indicate anywhere that the bridges do any kind of protocol conversion, as claimed herein.

Harris connects a device to a host using interface of a single bridging circuit. Harris itself teaches away from connecting multiple bridging circuits to a USB controller because it does not provide for addressing of individual devices connected to bridging circuits. This is further corroborated by the fact that Harris mentions nothing about connecting multiple bridges to the host. If it were possible to do so, Harris would have at least mentioned or suggested such a possibility in passing. Applicants respectfully request that the Examiner consider this evidence in examining the claims herein. If the Examiner disagrees, Applicants respectfully request that the Examiner specifically point to disclosure in Harris where multiple bridges can be supported.

Further, there is no motivation suggested by either reference to combine them. It is well settled that in order for a modification or combination of the prior art to be valid, the prior art itself must suggest the modification or combination, "...invention cannot be found obvious unless there was some **explicit** teaching or suggestion in the art to motivate one of ordinary skill to combine elements so as to create the same invention." *Winner International Royalty Corp. v. Wang*, No. 96-2107, 48 USPQ.2d 1139, 1140 (D.C.D.C. 1998) (emphasis added). "The prior art **must provide** one of ordinary skill in the art the **motivation** to make the proposed molecular modifications needed to arrive at the claimed compound." *In re Jones*, 958 F.2d 347, 21 USPQ.2d 1941, 1944 (Fed. Cir. 1992) (emphasis added).

Harris does not teach or suggest a mechanism for connecting multiple USB-to-IDE bridges to the host. Talati discloses nothing about connecting multiple USB-to-IDE bridges to the host or a USB controller. One of ordinary skill in the art would not look to, nor is taught by, such references for a way of determining how to support multiple bridges that function as protocol converters between multiple IDE devices and a USB controller that is connected to a host.

Despite the Examiner's suggestions, the claimed limitations are not mere duplication of working parts of the USB-to-IDE bridge, which is coupled to an IDE device, requiring only routine skill in the art. First, if that was indeed the case, at least the primary reference Harris would have

mentioned connecting multiple USB-to-IDE bridges to a USB controller. Clearly the Examiner is using hindsight here rather than indeed finding a reference that discloses such limitations. Further, the Examiner has not shown how the claimed limitations are mere duplication of working parts of the USB-to-IDE bridge, which is coupled to an IDE device, requiring only routine skill in the art. Where is that disclosed in the prior art? If the claimed limitations were a mere duplication, then why do not any of the reference even mention it in the passing?

There is no teaching in the prior art of connecting multiple IDE devices to multiple USB-to-IDE bridges that are connected to a USB controller. For at least these reasons, it is respectfully submitted that not prima facie case of obviousness has been established. Accordingly, rejection of Claim 1, and all claims dependent therefrom, should be withdrawn.

As per **Claim 3**, Harris and Talati do not disclose one or more USB hubs, each USB hub connected between two or more USB-to-IDE bridges and a USB controller, as claimed. Items 102 and 104 in Fig. 1 of Talati (relied upon by the Examiner) are not USB hubs as claimed (Talati says nothing about using USB or USB hubs). Items 102 and 104 are PHY controllers providing PHY layer protocol connection, not USB hubs. Nor does Harris mention use of USB hubs or need to USB hubs. If the claims are once again rejected, Applicant respectfully request that the Examiner point to disclosure in the references that teach one or more USB hubs, each USB hub connected between two or more USB-to-IDE bridges and a USB controller, as required by Claim 3.

As per **Claim 5**, Harris does not disclose that one or more IDE devices that are connected to bridges that are connected to a USB controller, can be connected/disconnected to/from the system while the system is operating, as claimed. Paragraph 25 of Harris (relied upon by the Examiner) says nothing about connecting/disconnecting one or more devices that are connected to bridges that are connected to a USB controller, as claimed.

As per **Claim 6**, Harris and Talati do not disclose that at least a third IDE device coupled to a corresponding USB-to-IDE bridge that is connected to a USB controller, can be connected/disconnected to/from the USB controller while the system is operating. Paragraph 25 of Harris (relied upon by the Examiner) says nothing about connecting/disconnecting a third IDE device that is connected to bridges that is connected to a USB controller, as claimed.

As per **Claim 7**, Harris and Talati do not disclose at least one USB hub connected between a number of the USB-to-IDE bridges and the USB controller whereby the processor can communicate with the IDE devices via the USB controller and the USB hub. Items 102 and 104 in Fig. 1 of Talati (relied upon by the Examiner) are not USB hubs as claimed (Talati says nothing about using USB or USB hubs). Items 102 and 104 are PHY controllers providing PHY layer protocol connection, not USB hubs. Nor does Harris mention use of USB hubs or need to USB hubs.

As per **Claim 8**, Harris does not disclose that one or more IDE devices can be disconnected from the system while the system is operating. Harris does not disclose that one or more IDE devices that are connected to bridges that are connected to a USB controller, can be disconnected from the system while the system is operating. Paragraph 25 of Harris (relied upon by the Examiner) says nothing about disconnecting one or more devices that are connected to bridges that are connected to a USB controller, as claimed.

As per **Claim 9**, Harris and Talati do not disclose that at least one additional IDE device coupled to a corresponding USB-to-IDE bridge can be connected to the hub while the system is operating. Harris does not disclose that IDE devices that are connected to bridges that are connected to a USB controller, can be disconnected from the system while the system is operating. Paragraph 25 of Harris (relied upon by the Examiner) says nothing about disconnecting devices that are connected to bridges that are connected to a USB controller. Talati and Harris are silent on USB hubs. Items 102 and 104 in Fig. 1 of Talati are not USB hubs as claimed (Talati says nothing about using USB or USB hubs. Nor does Harris mention use of USB hubs or need to USB hubs. As such,

Harris and Talati do not disclose that at least one additional IDE device coupled to a corresponding USB-to-IDE bridge can be connected to the hub while the system is operating

Claim 10 was rejected for essentially the same reasons as rejection of Claim 1. For at least the reasons provided in relation Claim 1, it is respectfully submitted that Claim 10 and all claims dependent therefrom should be allowed.

As per **Claim 12**, Harris does not disclose hot plugging/unplugging one or more IDE devices that are connected to bridges that are connected to a USB controller. Paragraph 25 of Harris (relied upon by the Examiner) says nothing about hot plugging/unplugging one or more devices that are connected to bridges that are connected to a USB controller, as claimed.

As per **Claim 13**, Harris and Talati do not disclose that one or more IDE devices that are connected to bridges that are connected to a USB controller, can be connected/disconnected to/from the system while the system is operating, as claimed. Paragraph 25 of Harris (relied upon by the Examiner) says nothing about connecting/disconnecting one or more devices that are connected to bridges that are connected to a USB controller, as claimed.

As per **Claim 14**, Harris and Talati do not disclose that at least a third IDE device coupled to a corresponding USB-to-IDE bridge that is connected to a USB controller, can be connected/disconnected to/from the USB controller while the system is operating. Paragraph 25 of Harris (relied upon by the Examiner) says nothing about connecting/disconnecting a third IDE device that is connected to bridges that is connected to a USB controller, as claimed.

As per **Claim 15**, Harris and Talati do not disclose providing at least one USB hub, connecting each hub to a USB controller, and connecting two or more USB-to-IDE bridges to each hub, such that each hub is connected between a USB controller and two or more USB-to-IDE bridges. There is no disclosure in the references of at least one USB hub connected between a

number of the USB-to-IDE bridges and the USB controller. Items 102 and 104 in Fig. 1 of Talati (relied upon by the Examiner) are not USB hubs as claimed (Talati says nothing about using USB or USB hubs). Items 102 and 104 are PHY controllers providing PHY layer protocol connection, not USB hubs. Nor does Harris mention use of USB hubs or need to USB hubs.

As per **Claim 16**, Harris and Talati do not disclose disconnecting one or more of the IDE devices from the system while the system is operating. Harris and Talati does not disclose that one or more IDE devices that are connected to bridges that are connected to a USB controller, can be disconnected from the system while the system is operating. Paragraph 25 of Harris (relied upon by the Examiner) says nothing about disconnecting one or more devices that are connected to bridges that are connected to a USB controller, as claimed.

Claim 18 was rejected for the same reasons as rejection of Claim 1. As such, Claim and claims dependent therefrom should be allowed for at least the reasons provided in relation to Claim 1.

As per **Claim 19**, Harris does not disclose a carrier for each IDE data storage device, such that each IDE disk drive and corresponding USB-to-IDE bridge are stored in the respective carrier. Fig. 3 of Harris (relied on by the Examiner) does not disclose that an IDE disk drive an corresponding USB-to-IDE bridge are stored in a carrier. Fig. 3 of Harris only shows a mass storage circuit board that carries the bridge chip 100 and disk drive *electronics* (not a storage device itself, such as disk drive, as claimed).

As per **Claim 20**, Harris and Talati do not disclose that one or more IDE storage devices can be disconnected from the system while the system is operating. The references do not disclose that that one or more IDE devices that are connected to bridges that are connected to a USB controller, can be disconnected from the system while the system is operating, as claimed. Paragraph 25 of

Harris (relied upon by the Examiner) says nothing about connecting/disconnecting one or more devices that are connected to bridges that are connected to a USB controller, as claimed.

As per **Claim 21**, Harris and Talati do not disclose that at least a third IDE disk device coupled to a corresponding USB-to-IDE bridge can be connected to the USB controller while the system is operating. The references do not disclose that at least a third IDE device coupled to a corresponding USB-to-IDE bridge can be connected to a USB controller, while the system is operating. Paragraph 25 of Harris (relied upon by the Examiner) says nothing about connecting a third IDE device that is connected to a bridge that is connected to a USB controller, as claimed.

As per **Claim 22**, Harris and Talati do not disclose at least one USB hub connected between a number of the USB-to-IDE bridges and the USB controller, whereby the processor can communicate with the IDE devices via the USB controller and the USB hub. Items 102 and 104 in Fig. 1 of Talati (relied upon by the Examiner) are not USB hubs as claimed (Talati says nothing about using USB or USB hubs). Items 102 and 104 are PHY controllers providing PHY layer protocol connection, not USB hubs. Nor does Harris mention use of USB hubs or need to USB hubs.

As per **Claim 23**, Harris and Talati do not disclose one or more USB hubs, each USB hub connected between two or more USB-to-IDE bridges and the USB controller. Items 102 and 104 in Fig. 1 of Talati (relied upon by the Examiner) are not USB hubs as claimed (Talati says nothing about using USB or USB hubs). Items 102 and 104 are PHY controllers providing PHY layer protocol connection, not USB hubs. Nor does Harris mention use of USB hubs or need to USB hubs. If the claims are once again rejected, Applicant respectfully request that the Examiner point to disclosure in the references that teach one or more USB hubs, each USB hub connected between two or more USB-to-IDE bridges and a USB controller, as required by Claim 23.

As per **Claim 24**, Harris and Talati do not disclose that at least one or more IDE storage devices can be disconnected from the system while the system is operating. The references do not disclose that that one or more IDE devices that are connected to bridges that are connected to a USB controller, can be disconnected from the system while the system is operating, as claimed. Paragraph 25 of Harris (relied upon by the Examiner) says nothing about connecting/disconnecting one or more devices that are connected to bridges that are connected to a USB controller, as claimed.

As per **Claim 25**, Harris and Talati do not disclose at least one additional IDE storage device coupled to a corresponding USB-to-IDE bridge can be connected to one of the USB hubs while the system is operating. As discussed, neither Harris nor Talati mention USB hubs, or use of USB hubs. Items 102 and 104 in Fig. 1 of Talati are not USB hubs as claimed (Talati says nothing about using USB or USB hubs). Items 102 and 104 are PHY controllers providing PHY layer protocol connection, not USB hubs. Nor does Harris mention use of USB hubs or need to USB hubs. Paragraph 25 of Harris (relied upon by the Examiner) says nothing about connecting an additional IDE device to a corresponding USB-to-IDE bridge to one of the USB hubs while the system is operating.

As per **Claim 26**, the references do not disclose that at least one additional IDE storage device coupled to a corresponding USB-to-IDE bridge and associated hub, can be connected to the USB controller while the system is operating. As discussed, the references are silent on USB hubs. Further, the references do not disclose an arrangement that comprises an IDE device connected to a USB-to-IDE bridge connected to a USB hub. Paragraph 25 of Harris (relied upon by the Examiner) says nothing about connecting such an arrangement to a USB controller in mid system operation.

As per **Claim 27**, the references do not disclose that at least one IDE storage device coupled to a corresponding USB-to-IDE bridge and associated hub, can be disconnected from the USB controller while the system is operating. As discussed, the references are silent on USB hubs.

Further, the references do not disclose an arrangement that comprises an IDE device connected to a USB-to-IDE bridge connected to a USB hub. Paragraph 25 of Harris (relied upon by the Examiner) says nothing about disconnecting connecting such an arrangement from a USB controller in mid system operation.

Rejection of Claims 2, 4, 11 under 35 U.S.C. 103(a) as being unpatentable over Harris in view Talati and further in view of Abramson is respectfully traversed since for at lese the following reasons, the references alone of in combination, do not disclose all of the claimed limitations.

As per **Claim 2**, as discussed Harris and Talati do not disclose all of the limitations of base Claim 1. Further, as the Examiner also states Harris and Talati do not all of the limitations of Claim 2. However, the Examiner interprets Abramson (Fig. 1) as showing a USB controller connected to a processor via a PCI bus. This interpretation of Abramson is respectfully traversed. First the Examiner has not pointed to the specific elements in Fig. 1 of Abramson that disclose such limitations. Further, in Fig. 1 of Abramson the processor 105 is not connected to the PCI bus (the processor 105 is connected to he host bridge 110). Further, the PCI bus 130 is not connected to any USB controller. Rather, the PCI bus 130 is connected to the host bridge 110, the buy interface unit 140 and the devices 135, none of which are USB controllers. As such, one of ordinary skill in the art would not look to the references to achieve the solution provided by the present invention. Further, the references themselves do suggest a motivation for the combination suggested by the Examiner. A PCI bus is not even mentioned in Harris or Talati.

As per **Claim 4**, as discussed Harris and Talati do not disclose all of the limitations of base Claim 1. In addition, Harris, Talati and Abramson do not disclose a plurality of USB controllers connected to the processor, wherein one or more USB-to-IDE bridges are connected to each USB controller via a USB bus, each USB-to-IDE bridge providing protocol conversion for communication between the corresponding IDE device and that USB controller, whereby the processor can communicate with the IDE devices via the USB controllers, as claimed. Further,

despite the Examiner's interpretation, it is respectfully submitted that Harris (paragraph 9, relied on by the Examiner) does not disclose one or more USB-to-IDE bridges are connected to each USB controller via a USB bus, each USB-to-IDE bridge providing protocol conversion for communication between the corresponding IDE device and that USB controller, whereby the processor can communicate with the IDE devices via the USB controllers. Harris, paragraph 9, simply states that: "Alternatively, a secondary board could be used to provide the translation function. In this embodiment, the secondary board includes the bridging circuit for converting ATA/ATAPI signals to USB signals. The secondary board receives the ATA/ATAPI signals from a mass storage device motherboard and outputs USB signals to the host motherboard." This is simply discussing placing the bridge circuit on one board and the disk drive electronics on another board. This has nothing to do with the claimed limitations.

Further, as the Examiner states, Harris and Talati do not disclose a plurality of USB controllers. Abramson (Figure 1) does no show a plurality of USB controllers connected to the processor 105, as claimed. There is no mention in Abramson of USB controllers, to each of which multiple USB-to-IDE bridges can be connected, as claimed. There is no motivation or suggestion by the references to combine them (indeed, Harris and Talati do no even mention one USB controller, let alone adding multiple USB controllers to them as the Examiner suggests). There is no disclosure, suggestion in the references that a processor can communicate with multiple IDE devices via multiple bridges via a plurality of USB controllers. The Examiner has not explained how the systems in the three references can be combined without extensive modification. It is respectfully submitted that the Examiner is simply using hindsight.

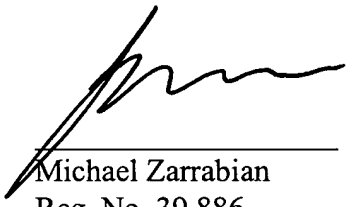
Claim 11 was rejected for the same reasons as rejection of Claim 2, and should therefore be allowed for at least the reasons provided in relation to Claim 2.

CONCLUSION

For the foregoing, and other, reasons Applicants believe that the rejected claims should be allowed. Reconsideration and allowance of the rejected claims are respectfully requested.

Please continue to direct all communications regarding the above-referenced patent application to the principal agent of record.

Respectfully Submitted,



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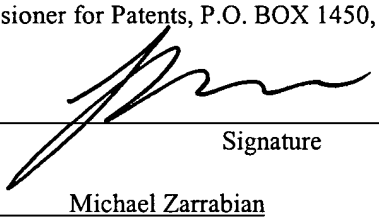
By 
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